IN THE CLAIMS

Listing of Claims:

1. (Currently amended) A method for submitting a test case for simulation of an integrated circuit design, comprising:

identifying a test case associated with a client;

verifying the test case at the client;

submitting the test case to a pre-initialized simulation server from the client;

associating text file based tasks of the test case to hardware description language (HDL) based tasks;

executing the test case on the pre-initialized simulation server;

communicating results from the test case execution to the client; and

executing a reset and initialization sequence at the pre-initialized simulation server to maintain the pre-initialized simulation server in an initialized state for a next test case.

2. (Original) The method of claim 1, wherein the method operation of verifying the test case at the client includes,

checking a syntax and a format of tasks defining the test case.

3. (Original) The method of claim 1, wherein the results are formatted as a results.log file.

4. (Original) The method of claim 1, further comprising:

providing a queue associated with the pre-initialized simulation server, the queue configured to store the test case.

5. (Original) The method of claim 1, wherein the method operation of communicating results from the test case execution to the client includes,

uninitializing the simulation server.

6. (Currently amended) The method of claim 1, wherein the method operation of executing the test case on the pre-initialized simulation server includes,

~~associating text file based tasks of the test case to hardware description language (HDL) based tasks; and~~

executing the HDL based tasks on a model of an integrated circuit design associated with the simulation server.

7. (Original) The method of claim 1, wherein the method operation of executing the test case on the pre-initialized simulation server includes,

translating each text based task associated with the verified test case to a compiled hardware description language (HDL) task.

8. (Original) The method of claim 7, wherein the compiled HDL task is stored on a storage media associated with the simulation server.

9. (Currently amended) A computer readable medium in which program instructions are stored, which instructions, when read by a computer, cause the computer to perform a method for minimizing simulation time overhead associated with the validation of an integrated circuit design, the method comprising:

executing a reset and initialization sequence at a server to maintain the server in an initialized state;

receiving a verified test case from a client in communication with the server;

associating text-file based tasks of the test case to hardware description language (HDL) based tasks;

executing the test case and recording results associated with execution of the test case;

communicating the results to the client; and

resetting the server to maintain the initialized state for receiving a next test case.

10. (Currently amended) The computer readable medium of claim 9, wherein executing the test case and recording results associated with execution of the test case includes,

~~associating text-file based tasks of the test case to hardware description language (HDL) based tasks; and~~

executing the HDL based tasks on a model of an integrated circuit design associated with the server.

11. (Previously presented) The computer readable medium of claim 9, wherein executing the test case and recording results associated with execution of the test case includes,

translating each of a text-based task associated with the verified test case to a compiled hardware description language (HDL) task.

12. (Previously presented) The computer readable medium of claim 9, wherein communicating the results to the client includes,

uninitializing the server.

13. (Previously presented) The computer readable medium of claim 9, wherein communicating the results to the client includes,

generating a results.log file.

14. (Currently amended) A system configured to minimize validation time associated with an integrated circuit design, comprising:

a client, the client configured to identify a test case for simulation with the integrated circuit design, the client further configured to generate a verified file from the test case, wherein the verified file includes text based tasks associated with hardware description language (HDL) based tasks;

a server in communication with the client; the server configured to maintain an initialized state, the server when in the initialized state configured to receive the HDL based tasks of the verified file from the client for execution, wherein after execution of the HDL based tasks of the verified file, the server is enabled to communicate results to the client and the server resets to the initialized state.

15. (Original) The system of claim 14, further comprising:

a storage medium in communication with the server, the storage medium configured to store compiled hardware description language based tasks corresponding to text based tasks associated with the verified file.

16. (Original) The system of claim 14, further comprising:

a network providing a communication pathway between the server and the client.

17. (Original) The system of claim 14, wherein the verified file includes a sequence of text-based tasks.

18. (Original) The system of claim 14, wherein the results are contained within a log-based file.

19. (Original) The system of claim 14, wherein the server further includes a queue, the queue configured to store a plurality of verified files.

20. (Original) The system of claim 14, wherein both the client and the server are general purpose computers.